Claims

1. An arrangement for vector permutation in a single-instruction multiple-data microprocessor, the arrangement comprising:
a permutation logic block coupled to receive and permutate vectors from at least one vector register according to control parameters;
a plurality of control registers, each coupled to selectively provide control parameters to the permutation logic block; and,
control means coupled between the plurality of control registers and the permutation logic block and arranged for selecting one of the plurality of control registers and for providing the control parameters from the selected one of the plurality of control registers to the permutation logic block.

2. A single-instruction multiple-data microprocessor vector permutation system comprising:
at least one vector register;
a permutation logic block coupled to receive and permutate vectors from the at least one vector register according to control parameters;
a plurality of control registers, each coupled to selectively provide control parameters to the permutation logic block; and,
control means coupled between the plurality of control registers and the permutation logic block and arranged for selecting one of the plurality of control registers and for providing the control parameters from the

selected one of the plurality of control registers to the permutation logic block.

3. The arrangement of claim 1 or system of claim 2 further comprising a negate block coupled to the control means and coupled to receive and selectively negate vectors from the permutation logic block according to the control parameters received from the control means, wherein the control parameters include permutation parameters and negate parameters.

4. The arrangement or system of any preceding claim wherein the control means includes at least one counter arranged to provide a sequential order for selecting one of the plurality of control registers.

5. A method for vector permutation in a single-instruction multiple-data microprocessor, the method comprising the steps of:
providing vectors to be permutated;
selecting one of a plurality of control registers, each control register containing parameters for determining permutation characteristics;
permutating the vectors according to the parameters of the selected control register.

6. The method of claim 5 wherein the control register parameters are also used for determining negate characteristics and the step of permutating further includes the step of selectively negating the vectors

according to the parameters of the selected control register.

7. The method of claim 5 or claim 6 wherein the step of selecting further includes the following of a sequential order of the plurality of control registers.

8. The arrangement or system of claim 4, or method of claim 7, wherein the sequential order includes automatic sequencing through a set of fixed control parameters.

9. The arrangement or system of claim 4, or method of claim 7, wherein the sequential order includes automatic sequencing through a set of programmable control parameters.

10. The arrangement, system or method of claims 4, 7, 8 or 9 wherein the sequential order is cyclical.

11. An arrangement for vector permutation in single-instruction multiple-data microprocessors substantially as hereinbefore described with reference to FIG. 2 of the accompanying drawings.

12. A system for vector permutation in single-instruction multiple-data microprocessors substantially as hereinbefore described with reference to FIG. 2 of the accompanying drawings.

13. A method for vector permutation in single-instruction multiple-data microprocessors substantially

as hereinbefore described with reference to FIG. 2 of the accompanying drawings.